PATENT ABSTRACTS OF JAPAN

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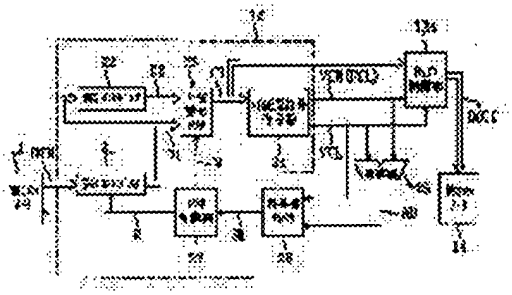
(54) DECODING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To accept the next code string with one-shift operation by shifting a code that consists of high order N bits within two N bits that are connected after successively acquiring each code word of variable and fixed length codes of parallel input data of N bits to high order side by the number of bits, that is equal to value which adds each word length of variable and fixed length codes.

SOLUTION: A high order filling shifter 23 shifts high order sixteen bits within thirty-two bits that combine parallel input data D1 and D2 of sixteen bits to be connected based on shift quantity M and outputs a code C1. An output controlling part 13A shifts the code C1 to a high order side, based on variable/fixed code length VCL/FCL and a code word VCW which are decoded by a variable length decoder 24. A shifter controller 27 supplies a quantity M, that is equal to addition value AD of those adders 25 to the shifter 23. By this means, the shifter 23 accepts the next code string with only one-shift operation and accelerates the operation.



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CLAIMS

[Claim(s)]
[Claim 1] It is the sign supplied as parallel input data which consists of an N bit. It has the regulation as which the symbolic language of a variable-length sign specifies the code length FCL of a consecutive fixed-length sign. And the code length addition means for being decryption equipment for decoding the sign which contains a variable-length sign at least, and adding the code length of said variable-length sign, and the code length FCL of said fixed-length sign, and supplying this aggregate value, The code length selection means for choosing either of the code length of said variable-length sign, and said aggregate value, and supplying this selection value, The parallel data which consist of a 2-N bit which is said parallel input data of a received single string The inside of the parallel data shifted to the high order side only M bits based on the amount M of shift assignment equal to the received selection value (M<=N), Decryption equipment characterized by having a decode means for supplying the 1st sign which consists of a high order N bit, and supplying respectively the symbolic language and code length who decoded said variable-length sign and were obtained.
[Claim 2] Decryption equipment characterized by having further an output-control means for generating the parallel output data with which only the number of bits equal to the code length of a variable-length sign who received the 1st received sign in decryption equipment according to claim 1 is shifted to a high order side, and consists of an N bit, and supplying these parallel output data.
[Claim 3] The sign selection means for choosing either in decryption equipment according to claim 1 among said 1st sign and 2nd sign which consist of an N bit respectively and which were received, and considering as the 3rd sign, and supplying this 3rd sign, The low order stuffing shift means for generating the 4th sign which only a N-FCL bit shifts the 3rd received sign to a low order side based on the code length FCL of a fixed-length sign who received, and consists of an N bit, and supplying this 4th sign, Shift only the number of bits equal to the code length of a variable-length sign who received the 1st received sign to a high order side, and it generates said 2nd sign. Decryption equipment which supplies this 2nd sign, supplies the code length FCL of a fixed-length sign who received to said low order stuffing shift means, and is characterized by having further an output-control means for outputting the parallel output data which consist of the 4th received sign.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the decryption equipment for decoding the sign containing a variable-length sign.
[0002]
[Description of the Prior Art] the symbol of an appearance probability with high variable length coding -- code length's short sign -- and by assigning code length's long sign to the low symbol of an appearance probability, respectively, code length's average is shortened and an overall sign yield is reduced. Therefore, since the code length changes with symbols, a variable-length sign will not be able to obtain the code length without decoding this variable-length sign.
[0003] The decoder for decoding the bit stream by which variable length coding was carried out is indicated by U.S. Pat. No. 5,173,695. The 1st and the 2nd storage means which cascade connection of [for this decoder to carry out the sequential storage of the input data respectively changed into the parallel data of bit width of face equal to the maximum code length of a variable-length sign] was carried out, The shifter for carrying out the sequential shift only of the number of bits of a request of the parallel data outputted from this storage means, The look-up table memory means for carrying out the sequential decode of the symbolic language of this variable-length sign by which only the number of bits equal to the code length of a variable-length sign is extracted from the high order side of the outputted this parallel data, The number of bits of a request equal to the code length of this variable-length sign is supplied to a shifter. and -- the case where the value which carried out sequential accumulation of this number of bits exceeds the bit width of face of the 1st storage means -- this -- it has the accumulator means for generating the read-out signal for transmitting the parallel data memorized by the 1st storage means to the 2nd storage means.
[0004]
[Problem(s) to be Solved by the Invention] However, in MPEG which is the international-standards method of picture compression, in case the above-mentioned conventional decoder decodes the sign train which encoded DC component of the DCT multipliers, it has a problem. This sign train has the regulation as which the symbolic language which consisted of a variable-length sign and a consecutive fixed-length sign, and decoded this variable-length sign specifies the code length of a consecutive fixed-length sign. As an example, a symbolic language explains ["4" and code length] the case where the sign train "1101001 XX--X" which consists of 16 bits containing the variable-length sign "110" which is "3", and the fixed-length sign "1001" whose code length is "4" is decoded. Here, X considers as the data which do not ask a value and a decoder makes 16 (=N) bit a batch. First, a variable-length sign "110" is decoded and a symbolic language "4" and code length "3" are obtained. The shifter which received the sign train "1101001 XX--X" to the 2nd supplies the parallel data "1001 XX--X" with which only the triplet shifted this sign train to the high order side based on code length "3", and an accumulator receives code length "3." The shifter which the accumulator received the code length "4" of a fixed-length sign, and supplied code length's accumulation value "7" (= 3+4), and received this accumulation value "7" to the 3rd shifts only 7 bits "1101001 XX--X" of sign trains to a high order side. An output serves as "XX--X" and this shifter will be in the condition which can accept the following sign train. Moreover, a fixed-length sign "1001" is obtained from parallel data "1001 XX--X" using the code length "4" of a fixed-length sign equal to the symbolic language "4" of the obtained variable-length sign. In order that a shifter may operate twice in the process of the 3 above-mentioned cycle, the number of cycles required for processing increases, and improvement in the speed is barred. Moreover, in case a fixed-length sign "1001" is decoded from the parallel data "1001 XX--X"

obtained by high order stuffing and a symbol is obtained, the cycle for omitting unnecessary data "XX--X" and making "1001" into low order stuffing is further needed.
[0005] This invention aims at offering the decryption equipment which can decode a variable-length sign and a fixed-length sign with the smaller number of cycles in view of the above-mentioned conventional trouble.
[0006]
[Means for Solving the Problem] The solution means which this invention provided in order to attain the above-mentioned purpose The decryption equipment for decoding a sign with the regulation as which it is supplied as parallel input data of N bit, and the symbolic language of a variable-length sign specifies the code length of a consecutive fixed-length sign The code length addition means for supplying the value adding the code length of a variable-length sign, and the code length of a fixed-length sign, The code length selection means for supplying the value chosen from either of this aggregate value and the code length of a variable-length sign, Based on the amount M of shift assignment equal to this selection value (M<=N), only M bits of parallel data which consist of a 2-N bit which connected a series of parallel input data are shifted to a high order side. And it considers as the configuration equipped with the decode means for supplying the sign which consists of a high order N bit of the shifted parallel data.
[0007] After obtaining the symbolic language of a sign to a variable-length sign and the symbolic language of a fixed-length sign which are supplied as parallel input data of N bit one by one by the above-mentioned configuration, only the number of bits equal to the value adding the code length of a variable-length sign and the code length of a fixed-length sign shifts to a high order side the sign which consists of a high order N bit among 2-N bits which connected this parallel input data. A decode means can change acceptance of the following sign train into a possible condition by 1 time of the shift action with this.
[0008]
[Embodiment of the Invention]
(1st operation gestalt) The 1st operation gestalt of the decryption equipment concerning this invention is explained, referring to drawing 1 and drawing 3 (a). Drawing 1 is the block diagram of the decryption equipment concerning the 1st operation gestalt of this invention. The decryption equipment of drawing 1 consists of the 1st memory 11, decode section 12, output-control section 13A, 2nd memory 14, adder 25, and code length selector 26.
[0009] The 1st memory 11 is a memory means for carrying out sequential supply of the parallel input data DIN which consists of 16 (=N) bit with the read-out signal R from the sign train stored beforehand. The decode section 12 is constituted by the 1st register 21, 2nd register 22, high order stuffing shifter 23, variable-length sign decoder 24, and shifter controller 27. The 1st register 21 is a storage means for supplying parallel input data DIN received and memorized to the high order stuffing shifter 23 or the 2nd register 22 according to the read-out signal R. The 2nd register 22 is a storage means for supplying the parallel data which received from the 1st register 21 and were memorized to the high order stuffing shifter 23. The high order stuffing shifter 23 the parallel data which consist of 32 (= 2Ns) bit which connected and generated the 1st input data D1 and 2nd input data D2 which were respectively received from the 1st and 2nd registers It is a high order stuffing shift means for supplying the 1st sign C1 which consists of a 16 (= N) bit high order among the parallel data shifted to the high order side only M bits according to the received amount M of shift assignment. The variable-length sign decoder 24 is a decoder for supplying the code length VCL and the symbolic language VCW of this variable-length sign which decoded and obtained the variable-length sign contained in the 1st received sign C1. An adder 25 is a code length addition means for adding the code length VCL of a variable-length sign who received, respectively, and the code length FCL of a fixed-length sign equal to the symbolic language VCW of this variable-length sign, and supplying an aggregate value AD. The code length selector 26 is a code length selection means for choosing either of the aggregate values AD and the code length VCL of a variable-length sign who received, respectively, and supplying the selection value SL. The shifter controller 27 is a shifter control means for supplying the read-out signal R, when the received selection value SL is accumulated, and the amount M of shift assignment is supplied and M (accumulation value) exceeds 16 (=N), and making a part for the excess into a new accumulation value. Output-control section 13A is an output-control means for outputting parallel output-data DOUT which consists of an N bit from which only the VCL bit shifted the 1st received sign to the high order side based on the code length VCL of a variable-length sign who received. The 2nd memory 14 is a storage means for memorizing received parallel output-data DOUT.
[0010] Actuation of the decryption equipment of drawing 1 is explained referring to drawing 3 (a). The case where it is the same as that of the example of the conventional technique is explained. Initial value of the amount M of shift

assignment is set to M= 0.
[0011] In 1 cycle eye of a shift shown in drawing 3 (a), the 1st memory 11 which received the read-out signal R supplies parallel input data DIN which consists of a 16-bit sign train "1101001 XX--X" to the 1st register 21. The 1st register 21 which received the read-out signal R supplies the memorized sign train to the 2nd register 22, and receives the following parallel input data DIN from the 1st memory 11 further. The high order stuffing shifter 23 receives the parallel data "1101001 XX--X" which are 16 bits of high orders among the parallel data which consist of 32 bits which connected the 1st input data D1 and 2nd input data D2 and which were memorized by the 2nd register 22. Furthermore, since the amount M of shift assignment is initial value "0", the high order stuffing shifter 23 does not shift these receptacle ****** parallel data, but it supplies the 1st sign C1 which consists of parallel data "1101001 XX--X." The variable-length sign decoder 24 decodes the variable-length sign "110" contained in this 1st sign C1, and supplies the code length "3" and the symbolic language "4" which were obtained. Based on the value "3" of the code length VCL of a variable-length sign, only a triplet shifts the 1st received sign C1 to a high order side, and output-control section 13A obtains parallel data "1001 XX--X", and writes a fixed-length sign "1001" in the 2nd memory 14 based on the value "4" of the code length FCL of a fixed-length sign further. An adder 25 adds the value "3" of the code length VCL of a variable-length sign, and the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, and supplies "7" which is this aggregate value AD. The code length selector 26 chooses "7" which is an aggregate value AD, and supplies it to the shifter controller 27.
[0012] In the two-cycle eye of a shift shown in drawing 3 (a), the shifter controller 27 supplies "7" which is the amount M of shift assignment equal to an aggregate value AD to the high order stuffing shifter 23. The high order stuffing shifter 23 shifts parallel data "1101001 XX--X" to a 7-bit high order side based on this amount M of shift assignment. By this, the output of the high order stuffing shifter 23 serves as "XX--X", and will be in the condition which can accept the following sign train.
[0013] According to the 1st operation gestalt, only by the high order stuffing shifter 23 operating once, as explained above, since decryption equipment will be in the condition which can accept the following sign train, it can reduce the number of cycles required for processing, and can attain improvement in the speed.
[0014] (2nd operation gestalt) The 2nd operation gestalt of the decryption equipment concerning this invention is explained, referring to drawing 2 and drawing 3 (b). The same sign is given to the same component as the 1st operation gestalt, and explanation is omitted. Drawing 2 is the block diagram of the decryption equipment concerning the 2nd operation gestalt of this invention. The decryption equipment of drawing 2 consists of the 1st memory 11, decode section 12, output-control section 13B, 2nd memory 14, adder 25, code length selector 26, sign selector 28, and low order stuffing shifter 29.
[0015] The sign selector 28 is a sign selection means for choosing either of the 1st sign C1 and the 2nd sign C2 which consist of 16 (=N) bit received, respectively, considering as the 3rd sign C3, and supplying this 3rd sign C3. The low order stuffing shifter 29 is a low order stuffing shift means for supplying the 4th sign C4 to which only the 16-FCL (N-FCL) bit shifted the 3rd received sign C3 to the low order side, and generated it based on the code length FCL of a fixed-length sign who received. The 2nd sign C2 from which only the VCL bit shifted the 1st received sign to the high order side based on the code length VCL of a variable-length sign who received is supplied, and output-control section 13B supplies the code length FCL of a fixed-length sign who received to the low order stuffing shifter 29, and is an output-control means for outputting parallel output-data DOUT of 16 (=N) bit which consists of the 4th received sign C4.
[0016] About actuation of the decryption equipment of drawing 2 , the case where the same sign train "1101001 XX--X" as the 1st operation gestalt is decoded is explained, referring to drawing 3 (b). Initial value of the amount M of shift assignment is set to M= 0. About the actuation which is common in the 1st operation gestalt, explanation is omitted suitably.
[0017] In 1 cycle eye of a shift shown in drawing 3 (b), the high order stuffing shifter 23 supplies the 1st sign C1 which consists of parallel data "1101001 XX--X." Based on the value "3" of the code length VCL of a variable-length sign, only a triplet shifts this 1st sign C1 of receptacle ****** to a high order side, and output-control section 13B supplies the 2nd sign C2 which consists of parallel data "1001 XX--X" containing a fixed-length sign "1001." An adder 25 adds the value "3" of the code length VCL of a variable-length sign, and the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, and supplies "7" which is an aggregate value AD. The code length selector 26 chooses "7" which is this aggregate value AD, and supplies it to

the shifter controller 27.
[0018] In the two-cycle eye of a shift shown in drawing 3 (b), the shifter controller 27 supplies "7" which is the amount M of shift assignment equal to an aggregate value AD to the high order stuffing shifter 23. The high order stuffing shifter 23 shifts parallel data "1101001 XX--X" to a 7-bit high order side based on "7" which is this amount M of shift assignment. The output of the high order stuffing shifter 23 serves as "XX--X" by this, and acceptance of the following sign train is attained. The sign selector 28 supplies this 3rd sign C3 that consists of parallel data "1001 XX--X" containing the fixed-length sign "1001" which chose the 2nd sign C2 among the 1st sign C1 and the 2nd sign C2, made the 3rd sign C3, and was made into high order stuffing.
[0019] In 3 cycle eye of a shift shown in drawing 3 (b), based on the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, only 12 (= 16-4) bit shifts the 3rd received sign C3 to a low order side, and the low order stuffing shifter 29 supplies the 4th sign C4 which consists of parallel data "00--01001." Output-control section 13B outputs parallel output-data DOUT which consists of parallel data "00--01001" containing the fixed-length sign "1001" which made this 4th sign C4 reception and low order stuffing. On the other hand, via the 2nd register 22, the high order stuffing shifter 23 receives the parallel data "1101001 XX--X" containing the following variable-length sign which follows "1101001" while having a symbolic language "m" with code length "n." Furthermore, the high order stuffing shifter 23 supplies the data which shifted and this shifted the data received based on "7" which is the amount M of shift assignment as following parallel data. By this, the high order stuffing shifter 23 outputs by making the following variable-length sign into high order stuffing. Like the following, the variable-length sign decoder 24 decodes a variable-length sign, and an adder 25 adds the value "n" of the code length VCL of a variable-length sign, and the value "m" of the code length FCL of the fixed-length sign specified by the symbolic language VCW of a variable-length sign, and supplies "n+m" which is an aggregate value AD. The code length selector 26 chooses this aggregate value AD, and supplies "n+m" which is this selection value SEL to the shifter controller 27.
[0020] As explained above, according to the 2nd operation gestalt, decryption equipment outputs parallel output-data DOUT which made the fixed-length sign low order stuffing only by the high order stuffing shifter 23 and the low order stuffing shifter 29 operating once each while being in the condition which can accept the following sign train. Therefore, decryption equipment is only the same number of cycles as the former, and can process even the cycle which makes a fixed-length sign low order stuffing.
[0021] In addition, in each operation gestalt explained above, when a variable-length sign is inputted continuously, the code length selector 26 chooses the corresponding code length VCL of a variable-length sign, and should just supply him. Moreover, a part of function of the microprocessor for controlling equipments other than decryption equipment can also be used as a function of output-control section 13A or 13B.
[0022]
[Effect of the Invention] According to the 1st decryption equipment of this invention, decryption equipment will be in the condition which can accept the following sign train by 1 time of the shift action. The high-speed decryption equipment which reduced the number of cycles required for processing is realizable with this.
[0023] Moreover, according to the 2nd decryption equipment of this invention, the parallel output data which decryption equipment changed into the condition which can accept the following sign train, and made the fixed-length sign low order stuffing by 2 times of shift actions are outputted. Since decryption equipment processes even the cycle which makes a fixed-length sign low order stuffing by the same count of a shift as the former by this, the decryption equipment high-speed one layer which finally reduced the number of cycles required for processing more is realizable.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the decryption equipment for decoding the sign containing a variable-length sign.

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PRIOR ART

[Description of the Prior Art] the symbol of an appearance probability with high variable length coding -- code length's short sign -- and by assigning code length's long sign to the low symbol of an appearance probability, respectively, code length's average is shortened and an overall sign yield is reduced. Therefore, since the code length changes with symbols, a variable-length sign will not be able to obtain the code length without decoding this variable-length sign. [0003] The decoder for decoding the bit stream by which variable length coding was carried out is indicated by U.S. Pat. No. 5,173,695. The 1st and the 2nd storage means which cascade connection of [for this decoder to carry out the sequential storage of the input data respectively changed into the parallel data of bit width of face equal to the maximum code length of a variable-length sign] was carried out, The shifter for carrying out the sequential shift only of the number of bits of a request of the parallel data outputted from this storage means, The look-up table memory means for carrying out the sequential decode of the symbolic language of this variable-length sign by which only the number of bits equal to the code length of a variable-length sign is extracted from the high order side of the outputted this parallel data, The number of bits of a request equal to the code length of this variable-length sign is supplied to a shifter. and -- the case where the value which carried out sequential accumulation of this number of bits exceeds the bit width of face of the 1st storage means -- this -- it has the accumulator means for generating the read-out signal for transmitting the parallel data memorized by the 1st storage means to the 2nd storage means.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to the 1st decryption equipment of this invention, decryption equipment will be in the condition which can accept the following sign train by 1 time of the shift action. The high-speed decryption equipment which reduced the number of cycles required for processing is realizable with this.
[0023] Moreover, according to the 2nd decryption equipment of this invention, the parallel output data which decryption equipment changed into the condition which can accept the following sign train, and made the fixed-length sign low order stuffing by 2 times of shift actions are outputted. Since decryption equipment processes even the cycle which makes a fixed-length sign low order stuffing by the same count of a shift as the former by this, the decryption equipment high-speed one layer which finally reduced the number of cycles required for processing more is realizable.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in MPEG which is the international-standards method of picture compression, in case the above-mentioned conventional decoder decodes the sign train which encoded DC component of the DCT multipliers, it has a problem. This sign train has the regulation as which the symbolic language which consisted of a variable-length sign and a consecutive fixed-length sign, and decoded this variable-length sign specifies the code length of a consecutive fixed-length sign. As an example, a symbolic language explains ["4" and code length] the case where the sign train "1101001 XX--X" which consists of 16 bits containing the variable-length sign "110" which is "3", and the fixed-length sign "1001" whose code length is "4" is decoded. Here, X considers as the data which do not ask a value and a decoder makes 16 (=N) bit a batch. First, a variable-length sign "110" is decoded and a symbolic language "4" and code length "3" are obtained. The shifter which received the sign train "1101001 XX--X" to the 2nd supplies the parallel data "1001 XX--X" with which only the triplet shifted this sign train to the high order side based on code length "3", and an accumulator receives code length "3." The shifter which the accumulator received the code length "4" of a fixed-length sign, and supplied code length's accumulation value "7" (= 3+4), and received this accumulation value "7" to the 3rd shifts only 7 bits "1101001 XX--X" of sign trains to a high order side. An output serves as "XX--X" and this shifter will be in the condition which can accept the following sign train. Moreover, a fixed-length sign "1001" is obtained from parallel data "1001 XX--X" using the code length "4" of a fixed-length sign equal to the symbolic language "4" of the obtained variable-length sign. In order that a shifter may operate twice in the process of the 3 above-mentioned cycle, the number of cycles required for processing increases, and improvement in the speed is barred. Moreover, in case a fixed-length sign "1001" is decoded from the parallel data "1001 XX--X" obtained by high order stuffing and a symbol is obtained, the cycle for omitting unnecessary data "XX--X" and making "1001" into low order stuffing is further needed.
[0005] This invention aims at offering the decryption equipment which can decode a variable-length sign and a fixed-length sign with the smaller number of cycles in view of the above-mentioned conventional trouble.

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MEANS

[Means for Solving the Problem] The solution means which this invention provided in order to attain the above-mentioned purpose The decryption equipment for decoding a sign with the regulation as which it is supplied as parallel input data of N bit, and the symbolic language of a variable-length sign specifies the code length of a consecutive fixed-length sign The code length addition means for supplying the value adding the code length of a variable-length sign, and the code length of a fixed-length sign, The code length selection means for supplying the value chosen from either of this aggregate value and the code length of a variable-length sign, Based on the amount M of shift assignment equal to this selection value (M<=N), only M bits of parallel data which consist of a 2-N bit which connected a series of parallel input data are shifted to a high order side. And it considers as the configuration equipped with the decode means for supplying the sign which consists of a high order N bit of the shifted parallel data.
[0007] After obtaining the symbolic language of a sign to a variable-length sign and the symbolic language of a fixed-length sign which are supplied as parallel input data of N bit one by one by the above-mentioned configuration, only the number of bits equal to the value adding the code length of a variable-length sign and the code length of a fixed-length sign shifts to a high order side the sign which consists of a high order N bit among 2-N bits which connected this parallel input data. A decode means can change acceptance of the following sign train into a possible condition by 1 time of the shift action with this.
[0008]
[Embodiment of the Invention]
(1st operation gestalt) The 1st operation gestalt of the decryption equipment concerning this invention is explained, referring to drawing 1 and drawing 3 (a). Drawing 1 is the block diagram of the decryption equipment concerning the 1st operation gestalt of this invention. The decryption equipment of drawing 1 consists of the 1st memory 11, decode section 12, output-control section 13A, 2nd memory 14, adder 25, and code length selector 26.
[0009] The 1st memory 11 is a memory means for carrying out sequential supply of the parallel input data DIN which consists of 16 (=N) bit with the read-out signal R from the sign train stored beforehand. The decode section 12 is constituted by the 1st register 21, 2nd register 22, high order stuffing shifter 23, variable-length sign decoder 24, and shifter controller 27. The 1st register 21 is a storage means for supplying parallel input data DIN received and memorized to the high order stuffing shifter 23 or the 2nd register 22 according to the read-out signal R. The 2nd register 22 is a storage means for supplying the parallel data which received from the 1st register 21 and were memorized to the high order stuffing shifter 23. The high order stuffing shifter 23 the parallel data which consist of 32 (= 2Ns) bit which connected and generated the 1st input data D1 and 2nd input data D2 which were respectively received from the 1st and 2nd registers It is a high order stuffing shift means for supplying the 1st sign C1 which consists of a 16 (= N) bit high order among the parallel data shifted to the high order side only M bits according to the received amount M of shift assignment. The variable-length sign decoder 24 is a decoder for supplying the code length VCL and the symbolic language VCW of this variable-length sign which decoded and obtained the variable-length sign contained in the 1st received sign C1. An adder 25 is a code length addition means for adding the code length VCL of a variable-length sign who received, respectively, and the code length FCL of a fixed-length sign equal to the symbolic language VCW of this variable-length sign, and supplying an aggregate value AD. The code length selector 26 is a code length selection means for choosing either of the aggregate values AD and the code length VCL of a variable-length sign who received, respectively, and supplying the selection value SL. The shifter controller 27 is a shifter control means for supplying the read-out signal R, when the received selection value SL is accumulated, and the

amount M of shift assignment is supplied and M (accumulation value) exceeds 16 (=N), and making a part for the excess into a new accumulation value. Output-control section 13A is an output-control means for outputting parallel output-data DOUT which consists of an N bit from which only the VCL bit shifted the 1st received sign to the high order side based on the code length VCL of a variable-length sign who received. The 2nd memory 14 is a storage means for memorizing received parallel output-data DOUT.

[0010] Actuation of the decryption equipment of drawing 1 is explained referring to drawing 3 (a). The case where it is the same as that of the example of the conventional technique is explained. Initial value of the amount M of shift assignment is set to M= 0.

[0011] In 1 cycle eye of a shift shown in drawing 3 (a), the 1st memory 11 which received the read-out signal R supplies parallel input data DIN which consists of a 16-bit sign train "1101001 XX--X" to the 1st register 21. The 1st register 21 which received the read-out signal R supplies the memorized sign train to the 2nd register 22, and receives the following parallel input data DIN from the 1st memory 11 further. The high order stuffing shifter 23 receives the parallel data "1101001 XX--X" which are 16 bits of high orders among the parallel data which consist of 32 bits which connected the 1st input data D1 and 2nd input data D2 and which were memorized by the 2nd register 22. Furthermore, since the amount M of shift assignment is initial value "0", the high order stuffing shifter 23 does not shift these receptacle ****** parallel data, but it supplies the 1st sign C1 which consists of parallel data "1101001 XX--X." The variable-length sign decoder 24 decodes the variable-length sign "110" contained in this 1st sign C1, and supplies the code length "3" and the symbolic language "4" which were obtained. Based on the value "3" of the code length VCL of a variable-length sign, only a triplet shifts the 1st received sign C1 to a high order side, and output-control section 13A obtains parallel data "1001 XX--X", and writes a fixed-length sign "1001" in the 2nd memory 14 based on the value "4" of the code length FCL of a fixed-length sign further. An adder 25 adds the value "3" of the code length VCL of a variable-length sign, and the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, and supplies "7" which is this aggregate value AD. The code length selector 26 chooses "7" which is an aggregate value AD, and supplies it to the shifter controller 27.

[0012] In the two-cycle eye of a shift shown in drawing 3 (a), the shifter controller 27 supplies "7" which is the amount M of shift assignment equal to an aggregate value AD to the high order stuffing shifter 23. The high order stuffing shifter 23 shifts parallel data "1101001 XX--X" to a 7-bit high order side based on this amount M of shift assignment. By this, the output of the high order stuffing shifter 23 serves as "XX--X", and will be in the condition which can accept the following sign train.

[0013] According to the 1st operation gestalt, only by the high order stuffing shifter 23 operating once, as explained above, since decryption equipment will be in the condition which can accept the following sign train, it can reduce the number of cycles required for processing, and can attain improvement in the speed.

[0014] (2nd operation gestalt) The 2nd operation gestalt of the decryption equipment concerning this invention is explained, referring to drawing 2 and drawing 3 (b). The same sign is given to the same component as the 1st operation gestalt, and explanation is omitted. Drawing 2 is the block diagram of the decryption equipment concerning the 2nd operation gestalt of this invention. The decryption equipment of drawing 2 consists of the 1st memory 11, decode section 12, output-control section 13B, 2nd memory 14, adder 25, code length selector 26, sign selector 28, and low order stuffing shifter 29.

[0015] The sign selector 28 is a sign selection means for choosing either of the 1st sign C1 and the 2nd sign C2 which consist of 16 (=N) bit received, respectively, considering as the 3rd sign C3, and supplying this 3rd sign C3. The low order stuffing shifter 29 is a low order stuffing shift means for supplying the 4th sign C4 to which only the 16-FCL (N-FCL) bit shifted the 3rd received sign C3 to the low order side, and generated it based on the code length FCL of a fixed-length sign who received. The 2nd sign C2 from which only the VCL bit shifted the 1st received sign to the high order side based on the code length VCL of a variable-length sign who received is supplied, and output-control section 13B supplies the code length FCL of a fixed-length sign who received to the low order stuffing shifter 29, and is an output-control means for outputting parallel output-data DOUT of 16 (=N) bit which consists of the 4th received sign C4.

[0016] About actuation of the decryption equipment of drawing 2 , the case where the same sign train "1101001 XX--X" as the 1st operation gestalt is decoded is explained, referring to drawing 3 (b). Initial value of the amount M of shift assignment is set to M= 0. About the actuation which is common in the 1st operation gestalt, explanation is omitted suitably.

[0017] In 1 cycle eye of a shift shown in drawing 3 (b), the high order stuffing shifter 23 supplies the 1st sign C1 which consists of parallel data "1101001 XX--X." Based on the value "3" of the code length VCL of a variable-length sign, only a triplet shifts this 1st sign C1 of receptacle ****** to a high order side, and output-control section 13B supplies the 2nd sign C2 which consists of parallel data "1001 XX--X" containing a fixed-length sign "1001." An adder 25 adds the value "3" of the code length VCL of a variable-length sign, and the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, and supplies "7" which is an aggregate value AD. The code length selector 26 chooses "7" which is this aggregate value AD, and supplies it to the shifter controller 27.

[0018] In the two-cycle eye of a shift shown in drawing 3 (b), the shifter controller 27 supplies "7" which is the amount M of shift assignment equal to an aggregate value AD to the high order stuffing shifter 23. The high order stuffing shifter 23 shifts parallel data "1101001 XX--X" to a 7-bit high order side based on "7" which is this amount M of shift assignment. The output of the high order stuffing shifter 23 serves as "XX--X" by this, and acceptance of the following sign train is attained. The sign selector 28 supplies this 3rd sign C3 that consists of parallel data "1001 XX--X" containing the fixed-length sign "1001" which chose the 2nd sign C2 among the 1st sign C1 and the 2nd sign C2, made the 3rd sign C3, and was made into high order stuffing.

[0019] In 3 cycle eye of a shift shown in drawing 3 (b), based on the value "4" of the code length FCL of the fixed-length sign specified by "4" which is the symbolic language VCW of a variable-length sign, only 12 (= 16-4) bit shifts the 3rd received sign C3 to a low order side, and the low order stuffing shifter 29 supplies the 4th sign C4 which consists of parallel data "00--01001." Output-control section 13B outputs parallel output-data DOUT which consists of parallel data "00--01001" containing the fixed-length sign "1001" which made this 4th sign C4 reception and low order stuffing. On the other hand, via the 2nd register 22, the high order stuffing shifter 23 receives the parallel data "1101001 XX--X" containing the following variable-length sign which follows "1101001" while having a symbolic language "m" with code length "n." Furthermore, the high order stuffing shifter 23 supplies the data which shifted and this shifted the data received based on "7" which is the amount M of shift assignment as following parallel data. By this, the high order stuffing shifter 23 outputs by making the following variable-length sign into high order stuffing. Like the following, the variable-length sign decoder 24 decodes a variable-length sign, and an adder 25 adds the value "n" of the code length VCL of a variable-length sign, and the value "m" of the code length FCL of the fixed-length sign specified by the symbolic language VCW of a variable-length sign, and supplies "n+m" which is an aggregate value AD. The code length selector 26 chooses this aggregate value AD, and supplies "n+m" which is this selection value SEL to the shifter controller 27.

[0020] As explained above, according to the 2nd operation gestalt, decryption equipment outputs parallel output-data DOUT which made the fixed-length sign low order stuffing only by the high order stuffing shifter 23 and the low order stuffing shifter 29 operating once each while being in the condition which can accept the following sign train. Therefore, decryption equipment is only the same number of cycles as the former, and can process even the cycle which makes a fixed-length sign low order stuffing.

[0021] In addition, in each operation gestalt explained above, when a variable-length sign is inputted continuously, the code length selector 26 chooses the corresponding code length VCL of a variable-length sign, and should just supply him. Moreover, a part of function of the microprocessor for controlling equipments other than decryption equipment can also be used as a function of output-control section 13A or 13B.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the decryption equipment concerning the 1st operation gestalt of this invention.
[Drawing 2] It is the block diagram of the decryption equipment concerning the 2nd operation gestalt of this invention.
[Drawing 3] (a) And (b) is drawing which explains the decode process by drawing 1 and the decryption equipment of drawing 2 , respectively.
[Description of Notations]
12 Decode Section (Decode Means)
13A, 13B Output-control section (output-control means)
25 Adder (Code Length Addition Means)
26 Code Length Selector (Code Length Selection Means)
28 Sign Selector (Sign Selection Means)
29 Low Order Stuffing Shifter (Low Order Stuffing Shift Means)
AD Aggregate value
C1 The 1st sign
C2 The 2nd sign
C3 The 3rd sign
C4 The 4th sign
DIN Parallel input data
DOUT Parallel output data
FCL Code length of a fixed-length sign
M The amount of shift assignment
SL Selection value
VCL Code length of a variable-length sign
VCW Symbolic language of a variable-length sign

[Translation done.]

* NOTICES *

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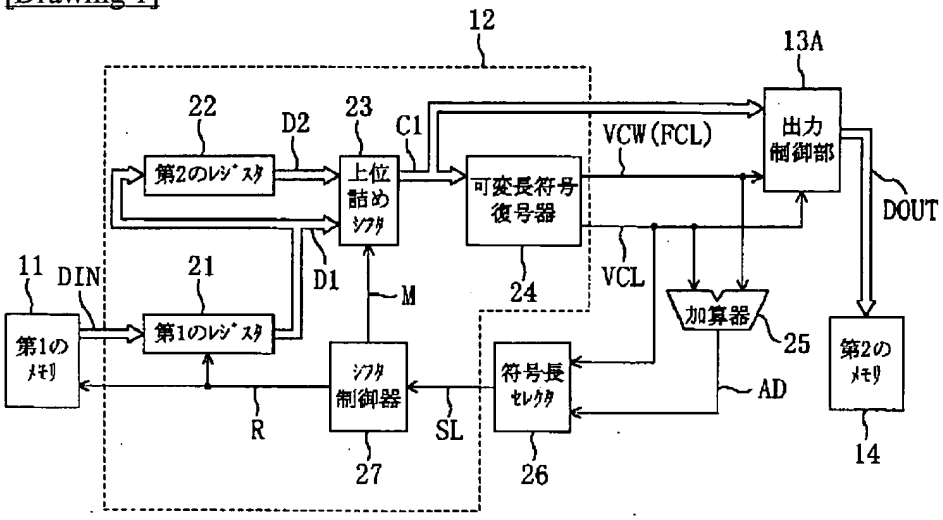
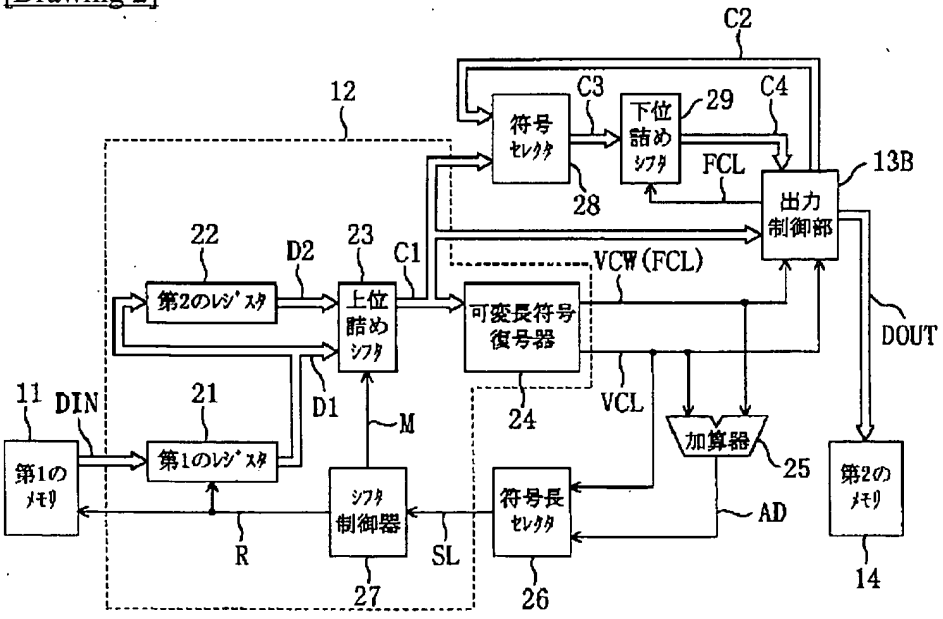
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



[Drawing 3]

ｻｲｸﾙ	第2のﾚｼﾞｽﾀの内容	第1のﾚｼﾞｽﾀの内容	上位詰めｼﾌﾄの出力	選択値	ｼﾌﾄ指定量
1	1101001XX･･･X	XX･････XX	1101001XX･･･X	7	0
2	1101001XX･･･X	XX･････XX	XX･･････････X	0	7

(a)

ｻｲｸﾙ	第2のﾚｼﾞｽﾀの内容	第1のﾚｼﾞｽﾀの内容	上位詰めｼﾌﾄの出力	下位詰めｼﾌﾄの出力	選択値	ｼﾌﾄ指定量
1	1101001XX･･･X	XX･････XX	1101001XX･･･X	XX･･･････X	7	0
2	1101001XX･･･X	XX･････XX	XX･･････････X	1001XX･･･X	0	7
3	1101001XX･･･X	XX･････XX	次のﾊﾟﾗﾚﾙﾃﾞｰﾀ	00･･･01001	n+m	7

n:次のﾊﾟﾗﾚﾙﾃﾞｰﾀの可変長符号の符号長
m:次のﾊﾟﾗﾚﾙﾃﾞｰﾀの固定長符号の符号長

(b)

[Translation done.]

09 918,129

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審査請求　未請求　請求項の数3　ＯＬ　（全 6 頁）

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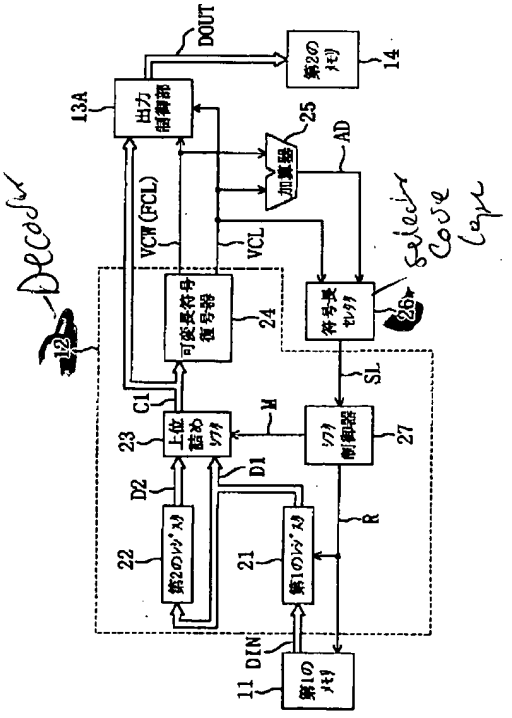
(54)【発明の名称】　復号化装置

(57)【要約】

【課題】　可変長符号の符号語が後続の固定長符号の符号長を指定する規則を持つ符号を復号するための、高速な復号化装置を提供する。

【解決手段】　Ｎビットのパラレル入力データＤＩＮとして順次受け取る符号を復号するための復号化装置であって、可変長符号の符号長ＶＣＬと固定長符号の符号長ＦＣＬとを加算するための加算器２５と、該加算値ＡＤと可変長符号の符号長ＶＣＬとのいずれかを選択値ＳＬとして選択するための符号長セレクタ２６と、該選択値ＳＬに等しいシフト指定量Ｍ（Ｍ≦Ｎ）に基づき一連のパラレル入力データＤＩＮよりなる２ＮビットをＭビット上位側へシフトし、該シフトされたデータの上位Ｎビットである第１の符号Ｃ１を供給し、かつ可変長符号を復号して符号長ＶＣＬと符号語ＶＣＷとを得るための復号部１２と、該第１の符号Ｃ１をＶＣＬビット上位側へシフトして出力するための出力制御部１３Ａとを備える。



1

【特許請求の範囲】

【請求項１】　Ｎビットよりなるパラレル入力データとして供給される符号であって、可変長符号の符号語が後続の固定長符号の符号長ＦＣＬを指定する規則を持ち、かつ少なくとも可変長符号を含む符号を復号するための復号化装置であって、

前記可変長符号の符号長と前記固定長符号の符号長ＦＣＬとを加算し、かつ該加算値を供給するための符号長加算手段と、

前記可変長符号の符号長と前記加算値とのいずれかを選択し、かつ該選択値を供給するための符号長選択手段と、

受け取った一連の前記パラレル入力データである２Ｎビットよりなるパラレルデータを、受け取った選択値に等しいシフト指定量Ｍ（Ｍ≦Ｎ）に基づいてＭビットだけ上位側へシフトしたパラレルデータのうち、上位Ｎビットよりなる第１の符号を供給し、かつ前記可変長符号を復号して得られた符号語と符号長とを各々供給するための復号手段とを備えたことを特徴とする復号化装置。

【請求項２】　請求項１記載の復号化装置において、受け取った第１の符号を受け取った可変長符号の符号長に等しいビット数だけ上位側へシフトしてＮビットよりなるパラレル出力データを生成し、かつ該パラレル出力データを供給するための出力制御手段を更に備えたことを特徴とする復号化装置。

【請求項３】　請求項１記載の復号化装置において、

各々Ｎビットよりなる受け取った前記第１の符号と第２の符号とのうちいずれかを選択して第３の符号とし、かつ該第３の符号を供給するための符号選択手段と、

受け取った固定長符号の符号長ＦＣＬに基づいて、受け取った第３の符号をＮ－ＦＣＬビットだけ下位側へシフトしてＮビットよりなる第４の符号を生成し、かつ該第４の符号を供給するための下位詰めシフト手段と、

受け取った第１の符号を受け取った可変長符号の符号長に等しいビット数だけ上位側へシフトして前記第２の符号を生成し、該第２の符号を供給し、受け取った固定長符号の符号長ＦＣＬを前記下位詰めシフト手段に供給し、受け取った第４の符号よりなるパラレル出力データを出力するための出力制御手段とを更に備えたことを特徴とする復号化装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、可変長符号を含む符号を復号するための復号化装置に関するものである。

【０００２】

【従来の技術】可変長符号化は、出現確率の高いシンボルに符号長の短い符号を、かつ出現確率の低いシンボルに符号長の長い符号をそれぞれ割り当てることにより、符号長の平均値を短くして全体的な符号発生量を低減する。したがって、可変長符号はシンボルによりその符号長が異なるので、該可変長符号を復号することにより初めてその符号長を得ることができる。

2

【０００３】米国特許第５，１７３，６９５号には、可変長符号化されたビットストリームを復号するための復号器が開示されている。該復号器は、可変長符号の最大符号長に等しいビット幅のパラレルデータに各々変換された入力データを順次記憶するためのカスケード接続された第１及び第２の記憶手段と、該記憶手段から出力されたパラレルデータを所望のビット数だけ順次シフトさせるためのシフタと、該出力されたパラレルデータの上位側から可変長符号の符号長に等しいビット数だけ抽出される該可変長符号の符号語を順次復号するためのルックアップテーブルメモリ手段と、該可変長符号の符号長に等しい所望のビット数をシフタに供給し、かつ該ビット数を順次累算した値が第１の記憶手段のビット幅を超えた場合には該第１の記憶手段に記憶されたパラレルデータを第２の記憶手段に転送するための読出信号を生成するための累算器手段とを備えている。

【０００４】

【発明が解決しようとする課題】しかしながら、上記従来の復号器は、例えば画像圧縮の国際標準方式であるＭＰＥＧにおいて、ＤＣＴ係数のうちのＤＣ成分を符号化した符号列を復号する際に問題を有する。該符号列は可変長符号と後続の固定長符号とからなり、かつ該可変長符号を復号した符号語が後続の固定長符号の符号長を指定する規則を持つ。例として、符号語が「４」かつ符号長が「３」である可変長符号「１１０」と、符号長が「４」である固定長符号「１００１」とを含む１６ビットよりなる符号列「１１０１００１ＸＸ…Ｘ」を復号する場合を説明する。ここで、Ｘは値を問わないデータとし、復号器は１６（＝Ｎ）ビットを処理単位とする。最初に、可変長符号「１１０」を復号して符号語「４」と符号長「３」とを得る。２番目に、符号列「１１０１００１ＸＸ…Ｘ」を受け取ったシフタは、符号長「３」に基づき該符号列を３ビットだけ上位側へシフトしたパラレルデータ「１００１ＸＸ…Ｘ」を供給し、かつ累算器は符号長「３」を受け取る。３番目に、累算器は固定長符号の符号長「４」を受け取って符号長の累算値「７」（＝３＋４）を供給し、該累算値「７」を受け取ったシフタは、符号列「１１０１００１ＸＸ…Ｘ」を７ビットだけ上位側へシフトする。該シフタは、出力が「ＸＸ…Ｘ」となり、次の符号列の受け入れが可能な状態になる。また、得られた可変長符号の符号語「４」に等しい固定長符号の符号長「４」を用いて、パラレルデータ「１００１ＸＸ…Ｘ」から固定長符号「１００１」を得る。上記３サイクルの過程においてシフタは２回動作するため、処理に必要なサイクル数が増えて高速化が妨げられる。また、上位詰めで得たパラレルデータ「１００１ＸＸ…Ｘ」から固定長符号「１００１」を復号してシンボルを得る際に、不要なデータ「ＸＸ…Ｘ」を切り捨

てて「１００１」を下位詰めにするためのサイクルが更に必要となる。

【０００５】本発明は、上記従来の問題点に鑑み、より少ないサイクル数で可変長符号と固定長符号とを復号できる復号化装置を提供することを目的とする。

【０００６】

【課題を解決するための手段】上記の目的を達成するために本発明が講じた解決手段は、Ｎビットのパラレル入力データとして供給され、かつ可変長符号の符号語が後続の固定長符号の符号長を指定する規則を持つ符号を復号するための復号化装置を、可変長符号の符号長と固定長符号の符号長とを加算した値を供給するための符号長加算手段と、該加算値と可変長符号の符号長とのいずれかより選択した値を供給するための符号長選択手段と、該選択値に等しいシフト指定量Ｍ（Ｍ≦Ｎ）に基づいて、一連のパラレル入力データを連結した２Ｎビットよりなるパラレルデータを Ｍビットだけ上位側へシフトし、かつシフトされたパラレルデータの上位Ｎビットよりなる符号を供給するための復号手段とを備えた構成としたものである。

【０００７】上記の構成により、Ｎビットのパラレル入力データとして供給される符号から可変長符号の符号語と固定長符号の符号語とを順次得た後に、該パラレル入力データを連結した２Ｎビットのうち上位Ｎビットよりなる符号を、可変長符号の符号長と固定長符号の符号長とを加算した値に等しいビット数だけ上位側へシフトする。このことにより復号手段は、１回のシフト動作によって次の符号列の受け入れを可能な状態にすることができる。

【０００８】

【発明の実施の形態】

（第１の実施形態）本発明に係る復号化装置の第１の実施形態を、図１及び図３（ａ）を参照しながら説明する。図１は、本発明の第１の実施形態に係る復号化装置の構成図である。図１の復号化装置は、第１のメモリ１１、復号部１２、出力制御部１３Ａ、第２のメモリ１４、加算器２５及び符号長セレクタ２６から構成される。

【０００９】第１のメモリ１１は、予め格納されている符号列から１６（＝Ｎ）ビットよりなるパラレル入力データＤＩＮを、読出信号Ｒにより順次供給するためのメモリ手段である。復号部１２は、第１のレジスタ２１、第２のレジスタ２２、上位詰めシフタ２３、可変長符号復号器２４及びシフタ制御器２７により構成される。第１のレジスタ２１は、受け取って記憶したパラレル入力データＤＩＮを、上位詰めシフタ２３又は第２のレジスタ２２に、読出信号Ｒに応じて供給するための記憶手段である。第２のレジスタ２２は、第１のレジスタ２１から受け取って記憶したパラレルデータを上位詰めシフタ２３に供給するための記憶手段である。上位詰めシフタ２３は、第１及び第２のレジスタから各々受け取った第１の入力データＤ１と第２の入力データＤ２とを連結して生成した３２（＝２Ｎ）ビットよりなるパラレルデータを、受け取ったシフト指定量Ｍに応じてＭビットだけ上位側へシフトしたパラレルデータのうち上位１６（＝Ｎ）ビットよりなる第１の符号Ｃ１を供給するための、上位詰めシフト手段である。可変長符号復号器２４は、受け取った第１の符号Ｃ１に含まれる可変長符号を復号して得た該可変長符号の符号長ＶＣＬと符号語ＶＣＷとを供給するための復号器である。加算器２５は、それぞれ受け取った、可変長符号の符号長ＶＣＬと、該可変長符号の符号語ＶＣＷに等しい固定長符号の符号長ＦＣＬとを加算して加算値ＡＤを供給するための符号長加算手段である。符号長セレクタ２６は、それぞれ受け取った加算値ＡＤと可変長符号の符号長ＶＣＬとのいずれかを選択して選択値ＳＬを供給するための符号長選択手段である。シフタ制御器２７は、受け取った選択値ＳＬを累算してシフト指定量Ｍを供給し、かつＭ（累算値）が１６（＝Ｎ）を超えた場合には読出信号Ｒを供給し、その過剰分を新たな累算値とするためのシフタ制御手段である。出力制御部１３Ａは、受け取った可変長符号の符号長ＶＣＬに基づいて、受け取った第１の符号をＶＣＬビットだけ上位側へシフトしたＮビットよりなるパラレル出力データＤＯＵＴを出力するための出力制御手段である。第２のメモリ１４は、受け取ったパラレル出力データＤＯＵＴを記憶するための記憶手段である。

【００１０】図１の復号化装置の動作について、図３（ａ）を参照しながら説明する。従来技術の例と同様の場合を説明する。シフト指定量Ｍの初期値をＭ＝０とする。

【００１１】図３（ａ）に示すシフトの１サイクル目において、読出信号Ｒを受け取った第１のメモリ１１は、１６ビットの符号列「１１０１００１ＸＸ…Ｘ」よりなるパラレル入力データＤＩＮを第１のレジスタ２１に供給する。読出信号Ｒを受け取った第１のレジスタ２１は、記憶している符号列を第２のレジスタ２２に供給し、更に第１のメモリ１１から次のパラレル入力データＤＩＮを受け取る。上位詰めシフタ２３は、第１の入力データＤ１と第２の入力データＤ２とを連結した３２ビットよりなるパラレルデータのうち上位１６ビットである、第２のレジスタ２２に記憶されたパラレルデータ「１１０１００１ＸＸ…Ｘ」を受け取る。更に上位詰めシフタ２３は、シフト指定量Ｍが初期値「０」であるから該受け取ったパラレルデータをシフトせず、パラレルデータ「１１０１００１ＸＸ…Ｘ」よりなる第１の符号Ｃ１を供給する。可変長符号復号器２４は、該第１の符号Ｃ１に含まれる可変長符号「１１０」を復号して、得られた符号長「３」と符号語「４」とを供給する。出力制御部１３Ａは、可変長符号の符号長ＶＣＬの値「３」に基づき、受け取った第１の符号Ｃ１を３ビットだけ上

位側へシフトしてパラレルデータ「１００１ＸＸ…Ｘ」を得、更に固定長符号の符号長ＦＣＬの値「４」に基づき、第２のメモリ１４に固定長符号「１００１」を書き込む。加算器２５は、可変長符号の符号長ＶＣＬの値「３」と、可変長符号の符号語ＶＣＷである「４」が指定した固定長符号の符号長ＦＣＬの値「４」とを加算し、該加算値ＡＤである「７」を供給する。符号長セレクタ２６は、加算値ＡＤである「７」を選択してシフタ制御器２７に供給する。

【００１２】図３（ａ）に示すシフトの２サイクル目において、シフタ制御器２７は、加算値ＡＤに等しいシフト指定量Ｍである「７」を上位詰めシフタ２３に供給する。上位詰めシフタ２３は、該シフト指定量Ｍに基づいて、パラレルデータ「１１０１００１ＸＸ…Ｘ」を７ビット上位側へシフトする。このことにより、上位詰めシフタ２３の出力は「ＸＸ…Ｘ」となり、次の符号列の受け入れが可能な状態になる。

【００１３】以上説明したように、第１の実施形態によれば、上位詰めシフタ２３が１回動作するだけで、復号化装置は次の符号列の受け入れが可能な状態になるため、処理に必要なサイクル数を削減して高速化を図ることができる。

【００１４】（第２の実施形態）本発明に係る復号化装置の第２の実施形態を、図２及び図３（ｂ）を参照しながら説明する。第１の実施形態と同一の構成要素には同一の符号を付し、説明を省略する。図２は、本発明の第２の実施形態に係る復号化装置の構成図である。図２の復号化装置は、第１のメモリ１１、復号部１２、出力制御部１３Ｂ、第２のメモリ１４、加算器２５、符号長セレクタ２６、符号セレクタ２８及び下位詰めシフタ２９から構成される。

【００１５】符号セレクタ２８は、それぞれ受け取った１６（＝Ｎ）ビットよりなる第１の符号Ｃ１と第２の符号Ｃ２とのいずれかを選択して第３の符号Ｃ３とし、該第３の符号Ｃ３を供給するための符号選択手段である。下位詰めシフタ２９は、受け取った固定長符号の符号長ＦＣＬに基づいて、受け取った第３の符号Ｃ３を１６－ＦＣＬ（Ｎ－ＦＣＬ）ビットだけ下位側へシフトして生成した第４の符号Ｃ４を供給するための下位詰めシフト手段である。出力制御部１３Ｂは、受け取った可変長符号の符号長ＶＣＬに基づいて、受け取った第１の符号をＶＣＬビットだけ上位側へシフトした第２の符号Ｃ２を供給し、受け取った固定長符号の符号長ＦＣＬを下位詰めシフタ２９に供給し、受け取った第４の符号Ｃ４よりなる１６（＝Ｎ）ビットのパラレル出力データＤＯＵＴを出力するための出力制御手段である。

【００１６】図２の復号化装置の動作について、図３（ｂ）を参照しながら、第１の実施形態と同様の符号列「１１０１００１ＸＸ…Ｘ」を復号する場合を説明する。シフト指定量Ｍの初期値をＭ＝０とする。第１の実

施形態と共通する動作については、適宜説明を省略する。

【００１７】図３（ｂ）に示すシフトの１サイクル目において、上位詰めシフタ２３は、パラレルデータ「１１０１００１ＸＸ…Ｘ」よりなる第１の符号Ｃ１を供給する。出力制御部１３Ｂは、可変長符号の符号長ＶＣＬの値「３」に基づき、該受け取った第１の符号Ｃ１を３ビットだけ上位側へシフトして、固定長符号「１００１」を含むパラレルデータ「１００１ＸＸ…Ｘ」よりなる第２の符号Ｃ２を供給する。加算器２５は、可変長符号の符号長ＶＣＬの値「３」と、可変長符号の符号語ＶＣＷである「４」が指定した固定長符号の符号長ＦＣＬの値「４」とを加算し、加算値ＡＤである「７」を供給する。符号長セレクタ２６は、該加算値ＡＤである「７」を選択してシフタ制御器２７に供給する。

【００１８】図３（ｂ）に示すシフトの２サイクル目において、シフタ制御器２７は、加算値ＡＤに等しいシフト指定量Ｍである「７」を上位詰めシフタ２３に供給する。上位詰めシフタ２３は、該シフト指定量Ｍである「７」に基づいて、パラレルデータ「１１０１００１ＸＸ…Ｘ」を７ビット上位側へシフトする。このことにより上位詰めシフタ２３の出力は「ＸＸ…Ｘ」となり、次の符号列の受け入れが可能になる。符号セレクタ２８は、第１の符号Ｃ１と第２の符号Ｃ２とのうち第２の符号Ｃ２を選択して第３の符号Ｃ３とし、上位詰めにした固定長符号「１００１」を含むパラレルデータ「１００１ＸＸ…Ｘ」よりなる該第３の符号Ｃ３を供給する。

【００１９】図３（ｂ）に示すシフトの３サイクル目において、下位詰めシフタ２９は、可変長符号の符号語ＶＣＷである「４」が指定した固定長符号の符号長ＦＣＬの値「４」に基づき、受け取った第３の符号Ｃ３を１２（＝１６－４）ビットだけ下位側へシフトして、パラレルデータ「００…０１００１」よりなる第４の符号Ｃ４を供給する。出力制御部１３Ｂは、該第４の符号Ｃ４を受け取り、下位詰めにした固定長符号「１００１」を含むパラレルデータ「００…０１００１」よりなる、パラレル出力データＤＯＵＴを出力する。一方、上位詰めシフタ２３は、第２のレジスタ２２を経由して、符号長「ｎ」と符号語「ｍ」とを持つと共に「１１０１００１」に後続する次の可変長符号を含む、パラレルデータ「１１０１００１ＸＸ…Ｘ」を受け取る。更に上位詰めシフタ２３は、シフト指定量Ｍである「７」に基づき受け取ったデータをシフトし、かつ該シフトしたデータを次のパラレルデータとして供給する。このことにより、上位詰めシフタ２３は次の可変長符号を上位詰めにして出力する。以下同様に、可変長符号復号器２４は可変長符号を復号し、加算器２５は、可変長符号の符号長ＶＣＬの値「ｎ」と、可変長符号の符号語ＶＣＷが指定した固定長符号の符号長ＦＣＬの値「ｍ」とを加算し、加算値ＡＤである「ｎ＋ｍ」を供給する。符号長セレクタ２

６は該加算値ＡＤを選択し、該選択値ＳＥＬである「ｎ＋ｍ」をシフタ制御器２７に供給する。

【００２０】以上説明したように、第２の実施形態によれば、上位詰めシフタ２３及び下位詰めシフタ２９が各１回動作するだけで、復号化装置は次の符号列の受け入れが可能な状態になると共に、固定長符号を下位詰めにしたパラレル出力データＤＯＵＴを出力する。したがって、復号化装置は従来と同じサイクル数だけで、固定長符号を下位詰めにするサイクルまでを処理できる。

【００２１】なお、以上説明した各実施形態において、可変長符号が連続して入力される場合には、符号長セレクタ２６は対応する可変長符号の符号長ＶＣＬを選択して供給すればよい。また、復号化装置以外の装置を制御するためのマイクロプロセッサの機能の一部を、出力制御部１３Ａ又は１３Ｂの機能として使用することもできる。

【００２２】

【発明の効果】本発明の第１の復号化装置によれば、１回のシフト動作によって、復号化装置は次の符号列の受け入れが可能な状態になる。このことによって、処理に必要なサイクル数を削減した高速な復号化装置を実現できる。

【００２３】また、本発明の第２の復号化装置によれば、２回のシフト動作によって、復号化装置は次の符号列の受け入れが可能な状態になり、かつ固定長符号を下位詰めにしたパラレル出力データを出力する。このことによって、復号化装置は従来と同じシフト回数で固定長符号を下位詰めにするサイクルまでを処理するので、最終的に処理に必要なサイクル数をより削減した一層高速な復号化装置を実現できる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態に係る復号化装置の構成図である。

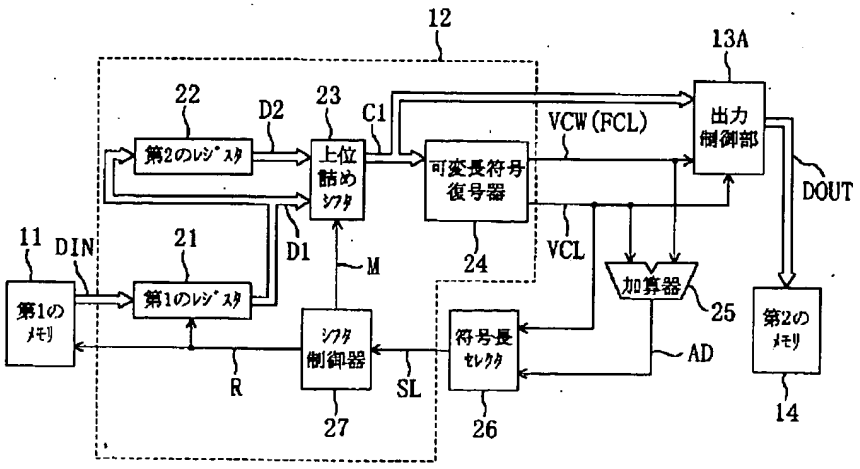
【図２】本発明の第２の実施形態に係る復号化装置の構成図である。

【図３】（ａ）及び（ｂ）は、それぞれ図１及び図２の復号化装置による復号過程を説明する図である。

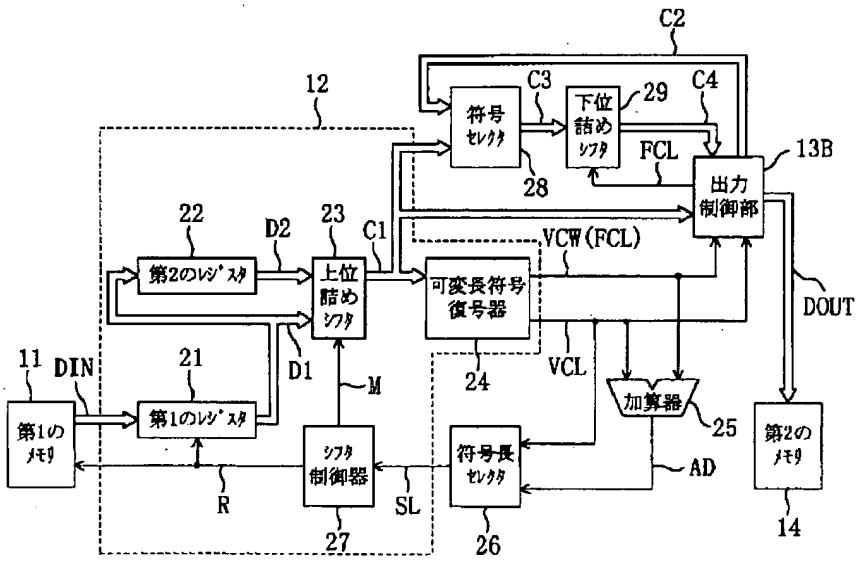
【符号の説明】

１２　復号部（復号手段）
１３Ａ，１３Ｂ　出力制御部（出力制御手段）
２５　加算器（符号長加算手段）
２６　符号長セレクタ（符号長選択手段）
２８　符号セレクタ（符号選択手段）
２９　下位詰めシフタ（下位詰めシフト手段）
ＡＤ　加算値
Ｃ１　第１の符号
Ｃ２　第２の符号
Ｃ３　第３の符号
Ｃ４　第４の符号
ＤＩＮ　パラレル入力データ
ＤＯＵＴ　パラレル出力データ
ＦＣＬ　固定長符号の符号長
Ｍ　シフト指定量
ＳＬ　選択値
ＶＣＬ　可変長符号の符号長
ＶＣＷ　可変長符号の符号語

【図１】



【図2】



【図3】

ｻｲｸﾙ	第2のﾚｼﾞｽﾀの内容	第1のﾚｼﾞｽﾀの内容	上位詰めｼﾌﾀの出力	選択値	ｼﾌﾄ指定量
1	1101001XX･･･X	XX･････XX	1101001XX･･･X	7	0
2	1101001XX･･･X	XX･････XX	XX･･････････X	0	7

(a)

ｻｲｸﾙ	第2のﾚｼﾞｽﾀの内容	第1のﾚｼﾞｽﾀの内容	上位詰めｼﾌﾀの出力	下位詰めｼﾌﾀの出力	選択値	ｼﾌﾄ指定量
1	1101001XX･･･X	XX･････XX	1101001XX･･･X	XX･･･････X	7	0
2	1101001XX･･･X	XX･････XX	XX･･････････X	1001XX･･･X	0	7
3	1101001XX･･･X	XX･････XX	次のﾊﾟﾗﾚﾙﾃﾞｰﾀ	00･･･01001	n+m	7

n:次のﾊﾟﾗﾚﾙﾃﾞｰﾀの可変長符号の符号長
m:次のﾊﾟﾗﾚﾙﾃﾞｰﾀの固定長符号の符号長

(b)